REMARKS

Claims 1, 24, and 29 are amended hereby. Claims 30-44 are canceled. Claims 45-46 are newly added. Accordingly, after entry of this Amendment, claims 1-26, 28-29, and 45-46 will remain pending.

In the Office Action dated April 26, 2006, the Examiner rejected claims 1-4, 6-23 under 35 U.S.C. § 102(b) as being anticipated by Buchanan et al. (U.S. Patent No. 6,245,616). Claims 24-26 and 28-29 were rejected under 35 U.S.C. § 103(a) as unpatentable over Buchanan et al. in view of Park et al. (U.S. Patent No. 6,825,518). Next, claim 30 was rejected under 35 U.S.C. § 103(a) as unpatentable over Buchanan et al. in view of Subramony et al. (U.S. Patent Application Publication No. 2003/0138562). Claims 31-42 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Buchanan et al. and Subramony et al. in view of Ikakura et al. (U.S. Patent No. 6,255,230). The Examiner also rejected claims 5 and 22 under 35 U.S.C. § 103(a) as unpatentable over Buchanan et al. in view of Solayappan et al. (U.S. Patent No. 5,997,642). Further, claims 43-44 were rejected under 35 U.S.C. § 103(a) as unpatentable over Buchanan et al. and Subramony et al. in view of Solayappan et al. The Applicant respectfully disagrees with each of these rejections and respectfully requests that the Examiner consider the following remarks in response to these rejections.

It is noted that, for the most part, the Examiner substituted Buchanan et al. for Niimi et al. to reject the claims. The Applicant, therefore, relies on the discussion presented by the previous submission, namely, the Response After Final filed on March 13, 2006. In particular, to simplify this Response and to avoid repetition of arguments previously presented that remain applicable to the present rejections, the Applicant incorporates the previous Response After Final herein by reference.

Buchanan et al. describes a method of forming an oxynitride film 22 by one of two methods. (Buchanan et al. at col. 6, lines 3-5.) In the first method, a standard thermal treatment process is employed involving at least one process gas of NO, NO_2 or NH_3, which is reacted with a silicon substrate 12, optionally in combination with an oxidizing gas such as O_2 or N_2O. (Buchanan et al. at col. 6, lines 5-9.) In a preferred embodiment for forming the oxynitride film 22, a clean surface of silicon is reacted with NO gas at a pressure between about 1 mTorr and about 20 atm, and a

temperature between about 500 °C and about 1200 °C. (Buchanan et al. at col. 6, lines 9-13.) A preferred range of reaction temperature is between about 650 °C and about 950 °C. (Buchanan et al. at col. 6, lines 13-15.) The second method involves a CVD process. (Buchanan et al. at col. 6, lines 15-18.)

After the formation of the oxynitride layer, Buchanan et al. describes the formation of an oxide spacer layer 32 between the oxynitride layer 22 and the silicon substrate 12. (Buchanan et al. at col. 6, lines 28-38.) Specifically, the silicon substrate is re-oxidized at an elevated temperature between about 500 °C and 1200 °C in an ambient containing an oxidizing agent and a halogenated species. (Buchanan et al. at col. 6, lines 28-31.) A substantially pure SiO_2 layer, which is not a high-k dielectric material, may then be formed on top of the oxynitride layer. (Buchanan et al. at col. 6, lines 24-27.) Following this methodology, the structure that results is illustrated in Fig. 2B: (1) a silicon substrate 12, (2) an oxide spacer layer 32 on top of the substrate 12, (3) an oxynitride layer 22 on top of the oxide spacer layer 32, and (4) a substantially pure SiO_2 layer 26 on top of the oxynitride layer 22. (Buchanan et al. at col. 6, lines 3-27.)

As is immediately apparent, this final structure differs from the structure resulting from the methodology of the present invention. Specifically, the present invention presents a method that results in the creation of the following structure: (1) a silicon substrate 100, (2) an oxynitride layer 102 on top of the substrate 100, and (3) a high-k layer 104 on top of the oxynitride layer 102. (See, e.g., the Specification at Fig. 1B.) In other words, the present invention results in a structure that excludes at least the oxide layer between the silicon substrate and the oxynitride layer and includes a high-k layer on top of the oxynitride layer. Since the method described by Buchanan et al. results in a different microstructure by including steps not required by the present invention, among other things, the Applicant respectfully submits that Buchanan et al. cannot anticipate claims 1-26, 28-29, and 45-46. Accordingly, the Applicant respectfully requests that the Examiner withdraw the rejection of the claims under 35 U.S.C. § 102(b).

Next, the Applicant addresses the rejection of claims 5 and 22 under 35 U.S.C. § 103(a) as unpatentable over Buchanan et al. in view of Solayappan et al. (U.S. Patent No. 5,997,642). As noted above, Buchanan et al. is wholly deficient as a

reference upon which to base a rejection of the claims now pending in this application. The Applicant has examined Solayappan et al. in detail and respectfully submits that Solayappan et al. does not cure the deficiencies noted with respect to Buchanan et al. and, therefore, cannot be combined with Buchanan et al. to render claims 5 and 22 obvious.

As noted above, Buchanan et al. is deficient as a reference at least because it describes a methodology that results in the creation of a microstructure including an oxide layer between the silicon substrate and the oxynitride layer and excluding at least a high-k layer atop the oxynitride layer. Solayappan et al. does not cure this deficiency because it does not describe a method consisting essentially of any of the features recited by claims 1-23 and 45. Instead, Solayappan et al. describes a method and apparatus for misted deposition of integrated circuit quality thin films. The film is formed from a liquid precursor, such as strontium bismuth tantalate. (Solayappan et al. at col. 7, lines 33-44.) No where does Solayappan et al. discuss at least a self-limiting thermal oxidation process for the formation of an oxynitride layer. Accordingly, the reference cannot be properly combined to render the claims unpatentable. As a result, the reference cannot be combined with Buchanan et al. in the manner suggested by the Examiner.

Turning to the rejection of claims 24-26 and 28-29 under 35 U.S.C. § 103(a), the Applicant respectfully submits that the combination of Buchanan et al. and Park et al. cannot render obvious any of claims 24-26, 28-29, and 46 as currently amended. Specifically, neither of these references describe or suggest a microstructure that consists essentially of a number of features including, among them, a substrate, an oxynitride layer on the substrate, and a high-k layer on the oxynitride layer. Accordingly, the Applicant respectfully requests that the Examiner withdraw the rejection of the claims under 35 U.S.C. § 103(a).

As noted above, Buchanan et al. describes a process that results in a microstructure with the following composition: (1) a silicon substrate 12, (2) an oxide spacer layer 32 on top of the substrate 12, (3) an oxynitride layer 22 on top of the oxide spacer layer 32, and (4) a substantially pure SiO_2 layer 26 on top of the oxynitride layer 22. (Buchanan et al. at col. 6, lines 3-27.) As noted, this structure

includes an oxide spacer layer 32 and excludes a high-k layer atop the oxynitride layer, both of which are included in claims 24-26, 28-29, and 46.

Park et al. does not assist the Examiner with a rejection of claims 24-26 and 28-29, because Park et al. describes that a silicon nitride layer 3 is formed on the lower (silicon) electrode 2. (Park et al. at col. 3, lines 40-45.) The silicon nitride layer 3 may be formed by a nitridation process using a plasma NH_3 treatment, a nitridation process using a thermal NH_3 treatment, or an N-LPCVD process. (Park et al. at col. 3, lines 45-50.) After the nitridation process, an oxidation treatment is performed to form the a silicon oxynitride layer 4 on the surface of the silicon nitride layer 3. (Park et al. at col. 3, lines 51-54.)

The resultant microstructure of the Park et al. disclosure is as follows: (1) a silicon substrate 1, (2) a lower electrode 2, possibly of doped silicon, on top of the substrate 1, (3) a silicon nitride layer 3 on top of the lower electrode 2, (4) a silicon oxynitride layer 4 on top of the silicon nitride layer 3, (5) a dielectric layer 5, possibly of Ta_2O_5, on top of the silicon oxynitride layer 4, and (6) an upper electrode 6, possibly of aluminum or doped silicon, on top of the dielectric layer 5. (See, e.g., Fig. 1E and col. 3, line 31, through col. 4, line 27.) As is immediately apparent, Park et al. includes, among other things, a lower electrode 2 and a silicon nitride layer 3 between the silicon substrate 1 and the silicon oxynitride layer 4, neither of which are recited by claims 24-26 and 28-29. At least for this reason, therefore, Park et al. does not assist the Examiner with a rejection of claims 24-26, 28-29, and 46. As a result, the Applicant respectfully requests that the Examiner withdraw the rejection of the claims under 35 U.S.C. § 103(a).

Since the Applicant has elected to cancel claims 30-44, the Applicant respectfully submits that the rejections of these claims has been rendered moot. Accordingly, the Applicant chooses not to address those rejections further.

Each of the rejections asserted by the Examiner having been addressed, the Applicant respectfully submits that claims 1-26, 28-29, and 45-46 are patentable over the references cited by the Examiner. Accordingly, the Applicant respectfully requests that the Examiner withdraw the rejections asserted against claims 1-26, 28-29, and 45-46 and pass this application quickly to issue.

If the Examiner believes a telephone conference would be helpful, he is invited to contact the undersigned at the telephone number given below.

Please charge any fees associated with the submission of this paper to Deposit Account Number 033975. The Commissioner for Patents is also authorized to credit any over payments to the above-referenced Deposit Account.

Respectfully submitted,

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